Solid State System Co., Ltd.

SSS1623A3/A4 USB Headset Controller Datasheet

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1. Product Overview

The SSS1623A3/A4 is a highly integrated USB audio controller with GPIO and MCU bus for function extension. SSS1623 features have mono 16bits ADC, stereo 16bits DAC, class AB earphone driver, microphone booster, embedded regulator, and is compliant with USB audio class v1.1, which make SSS1623 especially suitable for USB headset application. SSS1623 also integrates I2S and MCU interface, which provide more flexibility to connect to external codec or DSP for more function extension. SSS1623's functions can be programmed through external EEPROM (93C46), and vendor can customize its own USB VID/PID and serial number as well.

2. Product Features

USB

- Compliant with USB specification v2.0 full speed operation
- Compliant with USB audio device class specification v1.1
- Single 12MHz crystal to on-chip PLL for embedded USB transceiver

Audio

- Embedded 16-Bit Delta-Sigma mono ADC and stereo DAC
- Embedded I2S (master mode) interface for DAC/ADC
- In record mode, sampling rate for 8KHz, 11.025KHz, 22.05KHz, 32KHz, 44.1KHz, and 48KHz are supported
- Support 48KHz playback and recording sampling rate for headset application
- Support +20dB microphone boost (default) as AGC for USB audio driver control
- Support volume up, volume down, playback mute, recording mute for direct user control
- Support volume up, volume down, playback mute for Microsoft multimedia key
- Support embedded digital mixer function (SSS1623A4 only)
- Compatible with Win XP/Vista/7/8/8.1 and Mac system with OS's USB Audio driver

Peripheral

- Support EEPROM (93C46) programming interface for USB VID/PID, Product string and so on.
- External EEPROM register access optional by MCU (I2C interface) or USB HID interface

Power

- Embedded 5V to 3.3V, 1.8V and 2.3V output regulator from single external 5V USB bus power
- 1.8 V power for digital core, POR and audio PLL operation
- 3.3 V power for IO, oscillator, USB PLL, and ADC/DAC operation
- 2.3 V power for microphone bias
- Embedded stereo 16 bit DAC and 15 mW (32 ohm) class AB earphone driver

Package

- 48 LQFP, 64 LQFP, or dice

3. Ordering Information

Part Number	Package Type	Temperature Grade	Note
SSS1623A3-M6C	LQFP48	Commercial	Pb-free
SSS1623A3-M5C	LQFP64	Commercial	Pb-free
SSS1623A3-Y	Die	Commercial	Pb-free
SSS1623A4-M6C	LQFP48	Commercial	Pb-free
SSS1623A4-M5C	LQFP64	Commercial	Pb-free
SSS1623A4-Y	Die	Commercial	Pb-free

4. Electric Characteristics

Absolute Maximum Rating

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	VCC5A	-0.3 to +5.5	V
DC Input Voltage	Vin	-0.3 to +3.6	V
Operating Temperature	T_{opr}	0 to 70	^{0}C
Storage Temperature	T_{stg}	-20 to +120	^{0}C
Human Body Model ESD	HBM	2000	V
Machine Model ESD	MM	200	V

Operating conditions and regulator characteristics

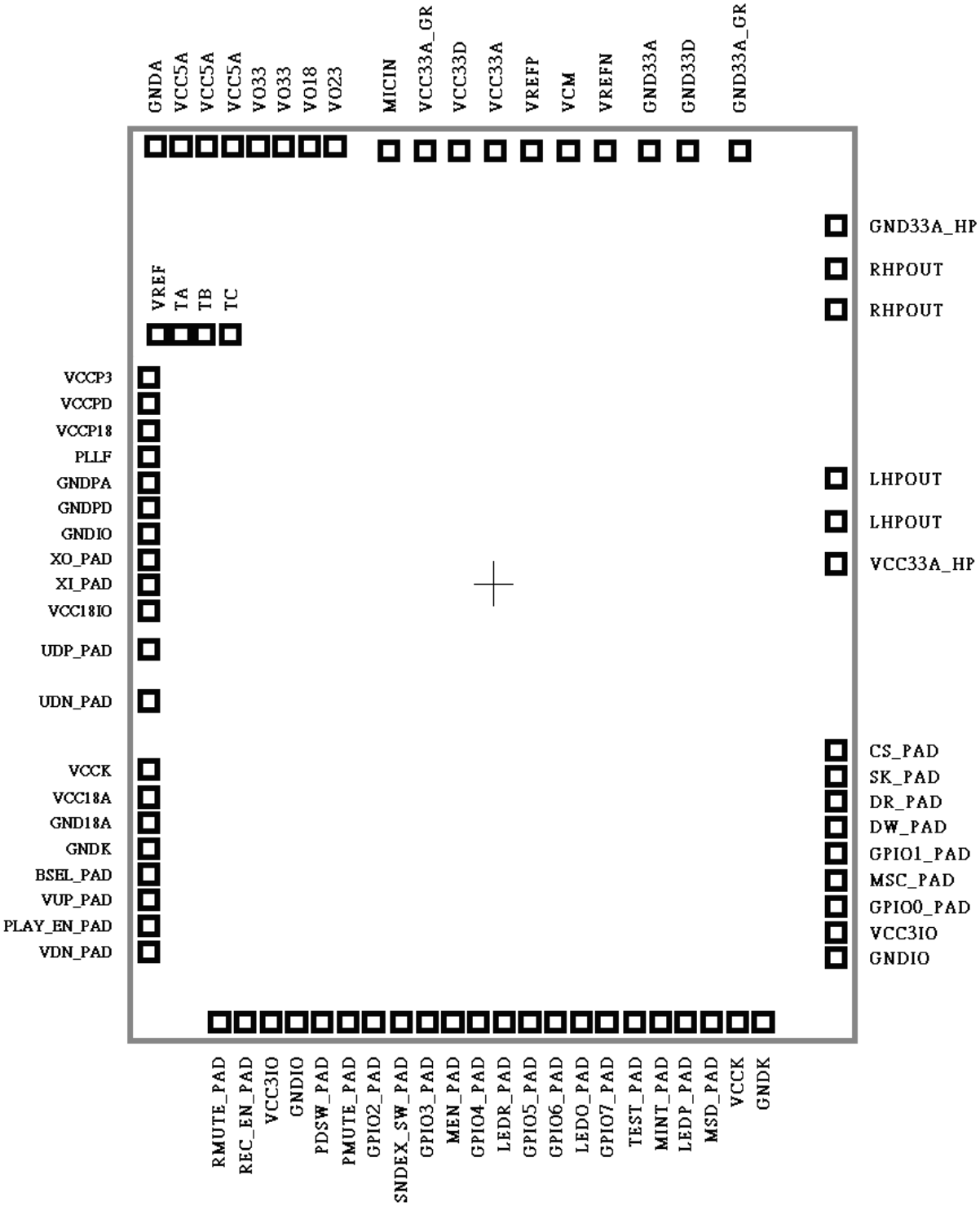
Symbol	Description	Condition	Min.	Typ.	Max.	unit
VCC5A	Power supply voltage		4.0	5.0	5.5	V
VO18	Regulator output voltage	VCC5A = 4 ~ 5 V	1.71	1.8	1.89	V
VO23	Microphone bias	VCC5A = 4 ~ 5 V	2.18	2.3	2.42	V
VO33	Regulator output voltage	VCC5A = 4 ~ 5 V	3.14	3.3	3.46	V
VCC3IO	3.3v power for IO		2.97	3.3	3.63	V
VCC33A_HP	3.3v power for Headphone Driver		2.7	3.3	3.6	V
VCC33A_GR	3.3v power for CODEC		2.7	3.3	3.6	V
VCCP3	3.3v power for audio PLL		2.7	3.3	3.6	V
VCCPD	PLL internal output voltage		1.62	1.8	1.98	V
VCCK	1.8V power for core logics		1.62	1.8	1.98	V
VCC18IO	1.8v power for crystal pads		1.62	1.8	1.98	V
Top	Operation ambient temperature		0		70	℃

Headphone output (Load = 16 Ω, 1 kHz Sine Wave, A-Weighted Filter)

Parameter	Condition	Min.	Typ.	Max.	unit
Full scale output voltage	0 dB	--	0.6*VCCA	--	Vpp
Maximum output power	RL = 16 Ω, VCC33A = 3.3 V	--	30	--	mW
Signal-to-noise ratio Input signal: 1kHz and -180dB (A-weighted)	VCC33A = 3.3 V , Fs=48kHz	--	-85	--	dB
Total harmonic distortion Input signal: 1 kHz	Fs=48kHz, VCC33A=3.3V, PO = 10 mW	--	0.1	--	%
Mute attenuation Input signal: 1 kHz and -0 dB (A-weighted)	--	--	-90	--	dB

5. Pin Description

5.1.1 Pad Location



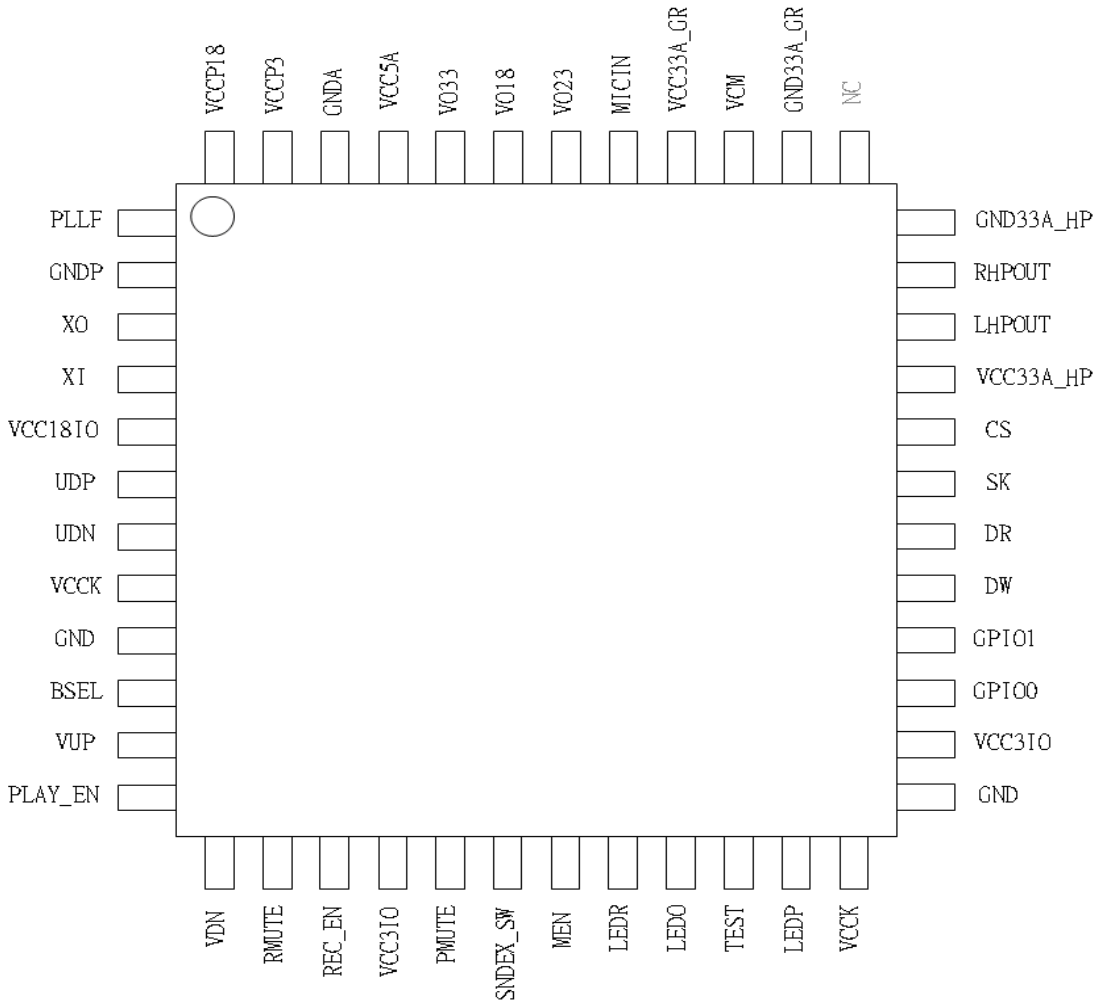
5.1.2 Pad Assignments

No.	Pad Name	Type	Description
1	VCCP3	P	3.3V power for PLL
2	VCCPD	P	1.8V power for PLL (Digital)
3	VCCP18	AO	1.8V output internal 3.3V → 1.8V regulator
4	PLLF	AO	Low pass filter pin for PLL
5	GNDPA	P	PLL ground
6	GNDPD	P	PLL ground (Digital)
7	GNDIO	P	Ground for Crystal Oscillator
8	XO_PAD	AO	output pin for 12MHz crystal
9	XI_PAD	AI	input pin for 12MHz crystal
10	VCC18IO	P	1.8v power for crystal oscillator pads
11	UDP_PAD	AIO	USB data D+
12	UDN_PAD	AIO	USB data D-
13	VCCK	P	Core power (1.8V)
14	VCC18A	P	1.8v power for USB PLL
15	GND18A	P	Ground for USB PLL
16	GNDK	P	Core ground
17	BSEL_PAD	I,PU	ROM Bank select 0:Bank 0 1:Bank 1
18	VUP_PAD	I,PU	Volume up
19	PLAY_EN_PAD	I,PU	Bonding option, different PID, and PLAY Enable 0 : disable 1 : enable
20	VDN_PAD	I,PU	Volume down
21	RMUTE_PAD	I,PU	Mute recording
22	REC_EN_PAD	I,PU	Bonding option, different PID, and REC Enable 0:disable 1:enable
23	VCC3IO	P	IO power (3.3V)
24	GNDIO	P	IO ground
25	PDSW_PAD	O,4mA	Power down switch control with external pull up resistor (for PMOS control)
26	PMUTE_PAD	I,PU	Mute playback
27	GPIO2_PAD	IO,PU,8mA	GPIO pin (SPI interface for external codec data control)
28	SNDEX_SW_PAD	I,PU	Sound expansion control enable/disable (switch mode) (Level trigger)
29	GPIO3_PAD	IO,PU,8mA	GPIO pin (I2S MCLK when audio path select to external)
30	MEN_PAD	I,PU	SSS1623A3 :Tied to ground SSS1623A4 : Mixer enable 1: enable 0: disable
31	GPIO4_PAD	IO,PU,8mA	GPIO pin (I2S BCLK when audio path select to external)
32	LEDR_PAD	IO,PZ,8mA	1. Recording mute LED indicator pin 2. Audio codec select: pull up – embedded codec; pull down – external codec
33	GPIO5_PAD	IO,PU,8mA	GPIO pin (I2S LRCLK when audio path select to external codec)

34	GPIO6_PAD	IO,PU,8mA	GPIO pin (I2S SDIN when audio path select to external codec)
35	LEDO_PAD	IO,PZ,8mA	LED Out (toggling for data transmit)(must be Pull Up)
36	GPIO7_PAD	IO,PU,8mA	GPIO pin (I2S SDOUT when audio path select to external codec)
37	TEST_PAD	I,PD	Test mode select pin 0: normal mode 1: test mode
38	MINT_PAD	O,4mA	External MCU interrupt pin
39	LEDP_PAD	IO,PD,16mA	Play mute indicator
40	MSD_PAD	IO,PU,8mA	External MCU serial bus data pin (after POR) or GPIO pin (by register programming)
41	VCCK	P	Core power (1.8V)
42	GNDK	P	Core ground
43	GNDIO	P	IO ground
44	VCC3IO	P	IO power (3.3V)
45	GPIO0_PAD	IO,PU,8mA	GPIO pin (SPI interface for external codec chip select control)
46	MSC_PAD	IO,PU,8mA	External MCU serial bus clock pin (after POR) or GPIO pin (by register programming)
47	GPIO1_PAD	IO,PU,8mA	GPIO pin (SPI interface for external codec clock control)
48	DW_PAD	I,PU	EEPROM interface data read from EEPROM
49	DR_PAD	IO,PD,4mA	EEPROM interface data write to EEPROM
50	SK_PAD	IO,PD,4mA	EEPROM interface clock
51	CS_PAD	IO,PD,4mA	EEPROM interface chip select
52	VCC33A_HP	P	Analog power pad of the headphone amplifier (3.3V)
53	LHPOUT	AO	Analog headphone out of left channel
54	LHPOUT	AO	Analog headphone out of left channel
55	RHPOUT	AO	Analog headphone out of right channel
56	RHPOUT	AO	Analog headphone out of right channel
57	GND33A_HP	P	Analog ground pad of the headphone amplifier
58	GND33A_GR	P	Analog ground pad
59	GND33D	P	Analog ground pad
60	GND33A	P	Analog ground pad
61	VREFN	P	Analog negative reference voltage negative
62	VCM	AO	Analog common mode voltage
63	VREFP	P	Analog positive reference voltage
64	VCC33A	P	Analog power pad (3.3V)
65	VCC33D	P	Analog power pad (3.3V)
66	VCC33A_GR	P	Analog power pad (3.3V)
67	MICIN	AI	Analog microphone input
68	VO23	P	2.3 V output for microphone bias (tristate in suspend mode)
69	VO18	P	1.8 V output voltage of the regulator
70	VO33	P	3.3 V output voltage of the regulator
71	VO33	P	3.3 V output voltage of the regulator
72	VCC5A	P	5 V power supply voltage
73	VCC5A	P	5 V power supply voltage

74	VCC5A	P	5 V power supply voltage
75	GNDA	P	Analog ground
76	VREF	Trimming pads	
77	TA	Trimming pads	
78	TB	Trimming pads	
79	TC	Trimming pads	

5.2.1 LQFP 48 Pin Chart

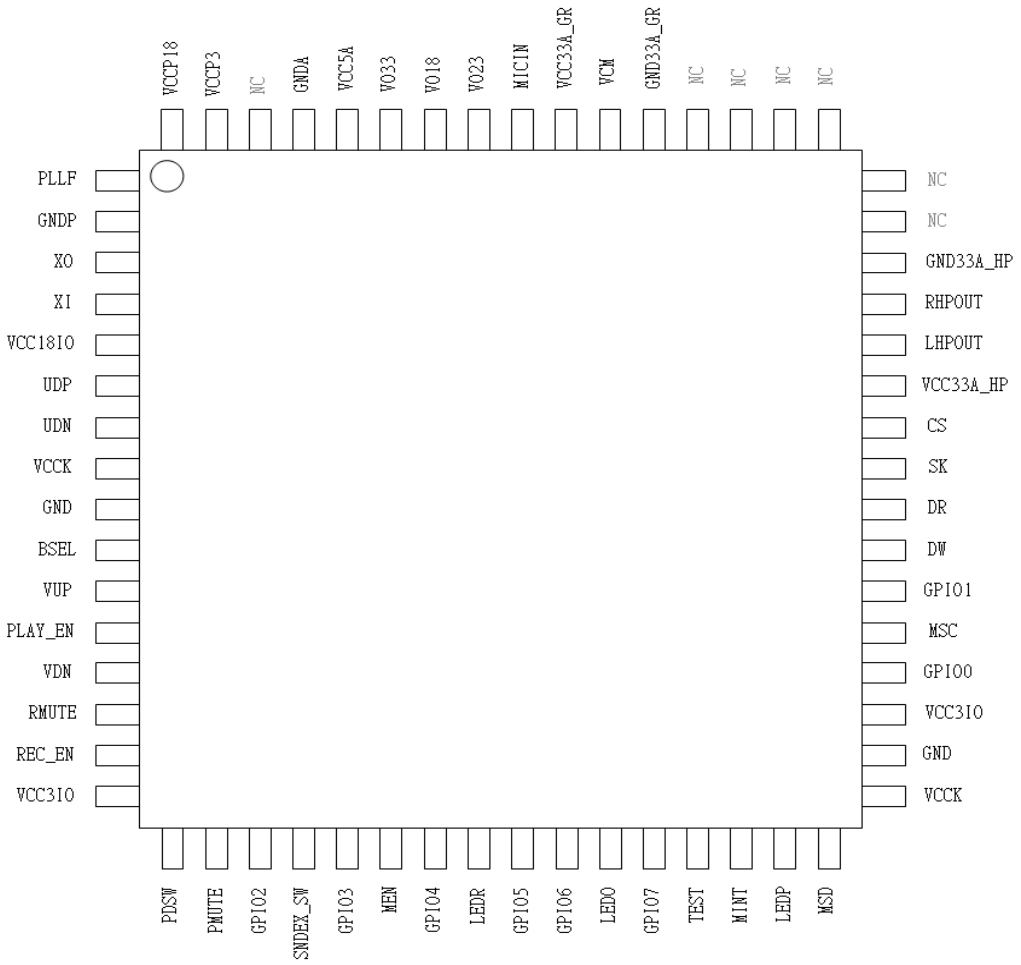


5.2.2 Pin Assignments

No.	Pin Name	Type	Description
1	PLLF	AO	Low pass filter for PLL
2	GNDP	P	Ground for Crystal Oscillator and PLL
3	XO	AO	output pin for 12MHz crystal
4	XI	AI	input pin for 12MHz crystal
5	VCC18IO	P	1.8v power for crystal oscillator pads
6	UDP	AIO	USB data D+
7	UDN	AIO	USB data D-
8	VCCK	P	Core power (1.8V)
9	GND	P	Ground
10	BSEL	I,PU	ROM Bank select 0:Bank 0 1:Bank 1
11	VUP	I,PU	Volume up
12	PLAY_EN	I,PU	Bonding option, different PID, and PLAY Enable 0 : disable 1 : enable

No.	Pin Name	Type	Description
13	VDN	I,PU	Volume down
14	RMUTE	I,PU	Mute recording
15	REC_EN	I,PU	Bonding option, different PID, and REC Enable 0:disable 1:enable
16	VCC3IO	P	IO power (3.3V)
17	PMUTE	I,PU	Mute playback
18	SNDEX_SW	I,PU	Sound expansion control enable/disable (switch mode) (level trigger)
19	MEN	I,PU	SSS1623A3 : Tied to ground SSS1623A4 : Mixer enable 1: enable 0: disable
20	LEDR	IO,PZ,8mA	Recording mute LED indicator pin; always pull up externally
21	LEDO	IO,PZ,8mA	Operation LED indicator, pull up externally
22	TEST	I,PD	Test mode select pin 0: normal mode 1: test mode
23	LEDP	IO,PD,16mA	Play mute indicator
24	VCCK	P	Core power (1.8V)
25	GND	P	ground
26	VCC3IO	P	IO power (3.3V)
27	GPIO0	IO,PU,8mA	GPIO pin
28	GPIO1	IO,PU,8mA	GPIO pin
29	DW	I,PU	EEPROM interface data read from EEPROM
30	DR	IO,PD,4mA	EEPROM interface data write to EEPROM
31	SK	IO,PD,4mA	EEPROM interface clock
32	CS	IO,PD,4mA	EEPROM interface chip select
33	VCC33A_HP	P	Analog power pad of the headphone amplifier (3.3V)
34	LHPOUT	AO	Analog headphone out of the left channel
35	RHPOUT	AO	Analog headphone out of the right channel
36	GND33A_HP	P	Analog ground pad of the headphone amplifier
37	--	--	NC
38	GND33A_GR	P	Analog ground pad
39	VCM	AO	Analog common mode voltage
40	VCC33A_GR	P	Analog power pad (3.3V)
41	MICIN	AI	Analog microphone input
42	VO23	P	2.3 V microphone bias; tristate in suspend mode
43	VO18	P	1.8 V output voltage of the regulator
44	VO33	P	3.3 V output voltage of the regulator
45	VCC5A	P	5 V power supply voltage
46	GNDA	P	Analog ground
47	VCCP3	P	3.3V power for audio PLL
48	VCCP18	AO	3.3V reference output for PLL internal 3.3V → 1.8V regulator

5.3.1 LQFP 64 Pin Chart



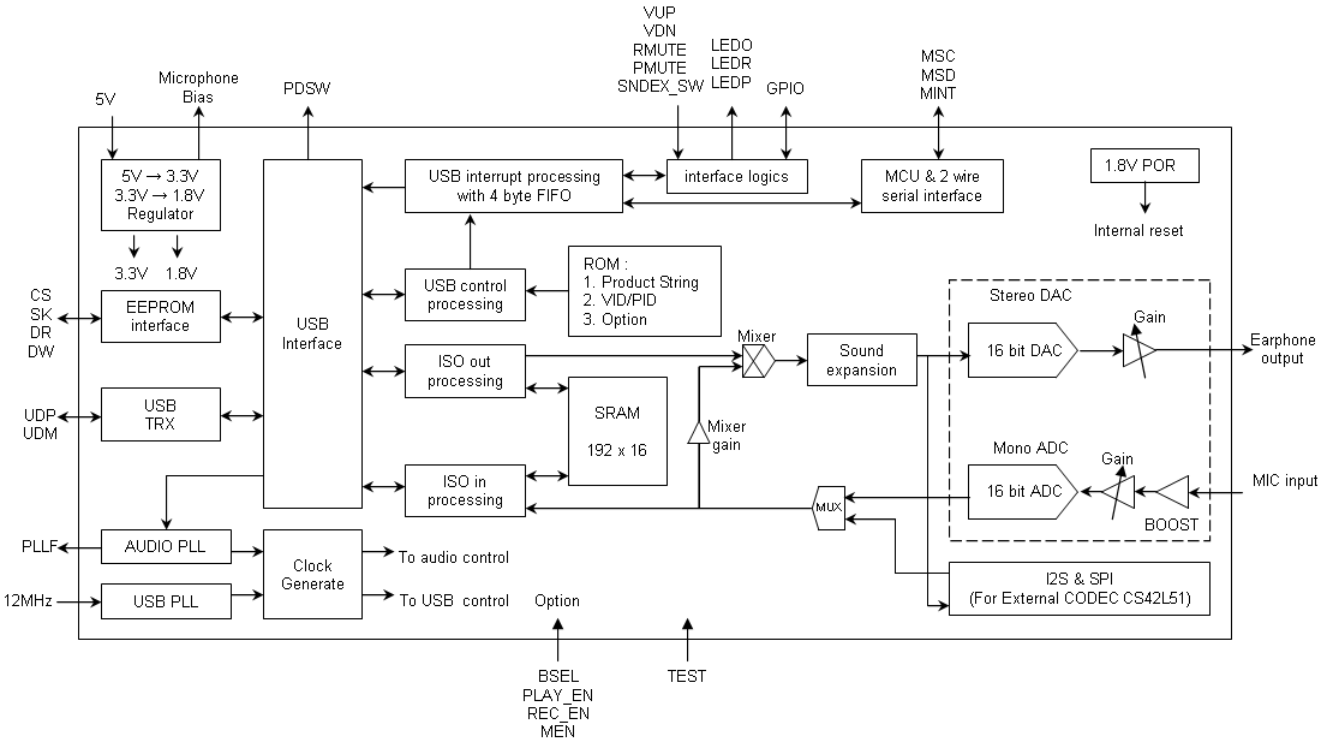
5.3.2 Pin Assignments

No.	Pin Name	Type	Description
1	PLLF	AO	Low pass filter for PLL
2	GNDP	P	Ground for Crystal Oscillator and PLL
3	XO	AO	output pin for 12MHz crystal
4	XI	AI	input pin for 12MHz crystal
5	VCC18IO	P	1.8v power for crystal oscillator pads
6	UDP	AIO	USB data D+
7	UDN	AIO	USB data D-
8	VCCK	P	Core power (1.8V)
9	GND	P	ground
10	BSEL	I,PU	ROM Bank select 0:Bank 0 1:Bank 1
11	VUP	I,PU	Volume up
12	PLAY_EN	I,PU	Bonding option, different PID, and PLAY Enable 0 : disable 1 : enable
13	VDN	I,PU	Volume down
14	RMUTE	I,PU	Mute recording

No.	Pin Name	Type	Description
15	REC_EN	I,PU	Bonding option, different PID, and REC Enable 0:disable 1:enable
16	VCC3IO	P	IO power (3.3V)
17	PDSW	O,4mA	Power down switch control (for PMOS polarity)
18	PMUTE	I,PU	Mute playback
19	GPIO2	IO,PU,8mA	GPIO pin (SPI interface for external codec data control)
20	SNDEX_SW	I,PU	Sound expansion control enable/disable (Level trigger)
21	GPIO3	IO,PU,8mA	GPIO pin (I2S MCLK when audio path set to external codec)
22	MEN	I,PU	SSS1623A3 : Tied to ground SSS1623A4 : Mixer enable 1: enable 0: disable
23	GPIO4	IO,PU,8mA	GPIO pin (I2S BCLK when audio path set to external codec)
24	LEDR	IO,PZ,8mA	1. Recording mute LED indicator pin 2. Audio codec select: pull up – embedded codec; pull down – external codec
25	GPIO5	IO,PU,8mA	GPIO pin (I2S LRCLK when audio path set to external codec)
26	GPIO6	IO,PU,8mA	GPIO pin (I2S SDIN when audio path set to external codec)
27	LEDO	IO,PZ,8mA	Operation LED indicator, pull up externally
28	GPIO7	IO,PU,8mA	GPIO pin (I2S SDOUT when audio path set to external codec)
29	TEST	I,PD	Test mode select pin 0: normal mode 1: test mode
30	MINT	O,4mA	External MCU interrupt pin
31	LEDP	IO,PD,16mA	Play mute indicator
32	MSD	IO,PU,8mA	External MCU serial bus data pin (after POR) or GPIO pin (by register programming)
33	VCCK	P	Core power (1.8V)
34	GND	P	Ground
35	VCC3IO	P	IO power (3.3V)
36	GPIO0	IO,PU,8mA	GPIO pin (SPI interface for external codec chip select control)
37	MSC	IO,PU,8mA	External MCU serial bus clock pin (after POR) or GPIO pin (by register programming)
38	GPIO1	IO,PU,8mA	GPIO pin (SPI interface for external codec clock control)
39	DW	I,PU	EEPROM interface data read from EEPROM
40	DR	IO,PD,4mA	EEPROM interface data write to EEPROM
41	SK	IO,PD,4mA	EEPROM interface clock
42	CS	IO,PD,4mA	EEPROM interface chip select
43	VCC33A_HP	P	Analog power pad of the headphone amplifier (3.3V)
44	LHPOUT	AO	Analog headphone out of the left channel
45	RHPOUT	AO	Analog headphone out of the right channel
46	GND33A_HP	P	Analog ground pad of the headphone amplifier
47	NC	--	NC
48	NC	--	NC
49	NC	--	NC

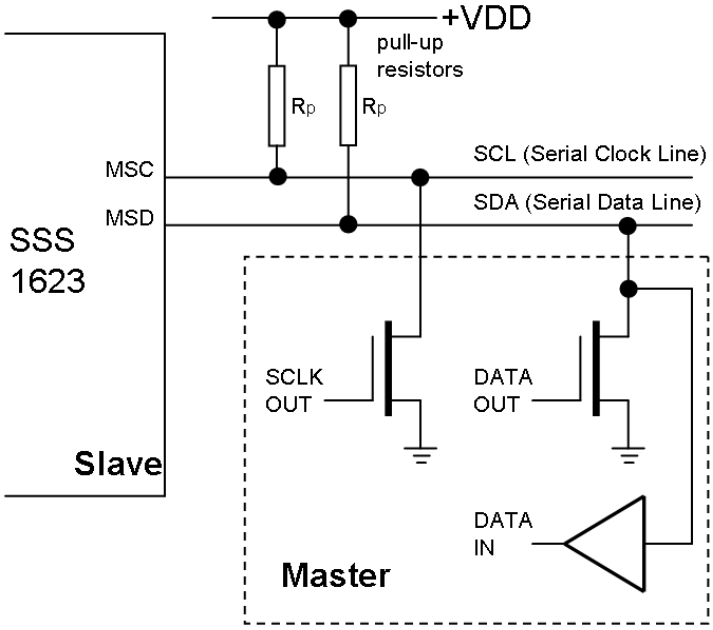
50	NC	--	NC
51	NC	--	NC
52	NC	--	NC
53	GND33A_GR	P	Analog ground pad
54	VCM	AO	Analog common mode voltage
55	VCC33A_GR	P	Analog power pad (3.3V)
56	MICIN	AI	Analog microphone input
57	VO23	P	2.3 V output for microphone bias; tristate in suspend mode
58	VO18	P	1.8 V output voltage of the regulator
59	VO33	P	3.3 V output voltage of the regulator
60	VCC5A	P	5 V power supply voltage
61	GNDA	P	Analog ground
62	NC	--	NC
63	VCCP3	P	3.3V power for audio PLL
64	VCCP18	AO	3.3V reference output for PLL internal 3.3V → 1.8V regulator

6. Block Diagram and Descriptions

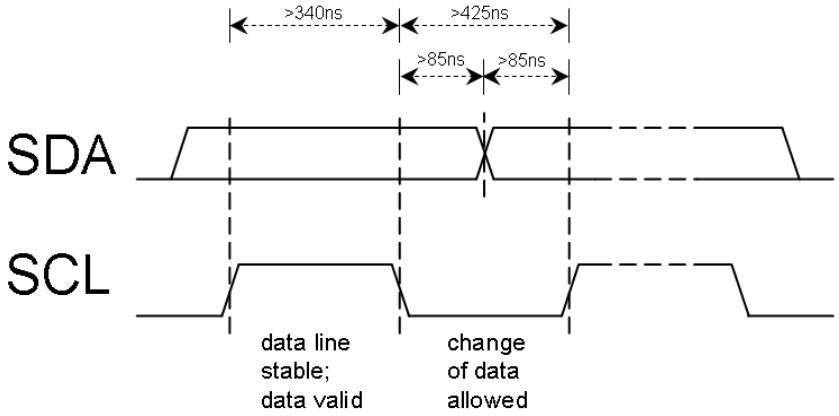


- **MCU 2 Wire Serial Bus**

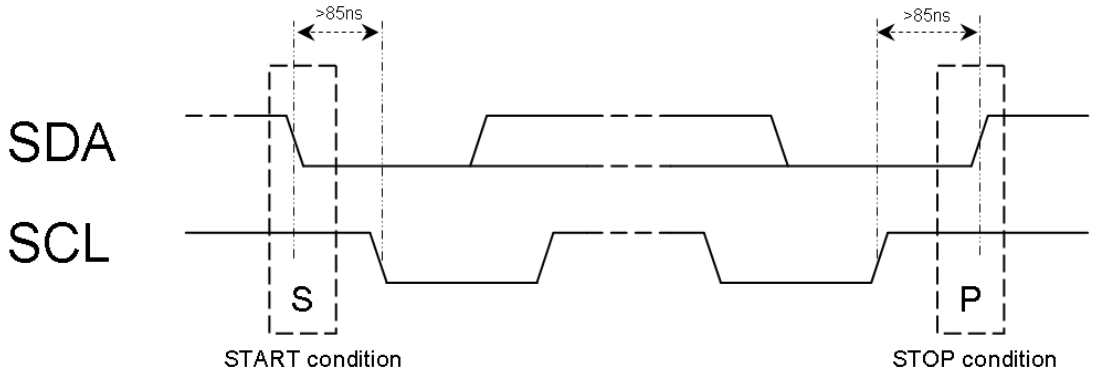
6.1 Connection of the devices to the 2 wire serial bus



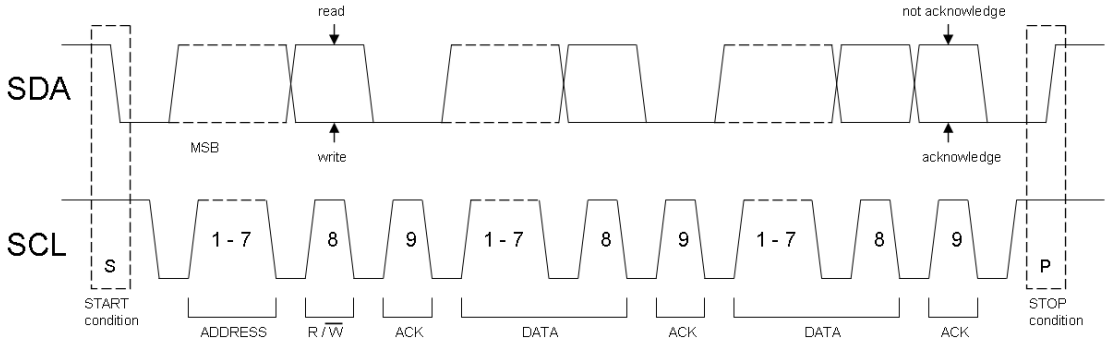
6.2 Bit transfer on the SSS1623 2 wire serial bus



6.3 START and STOP conditions

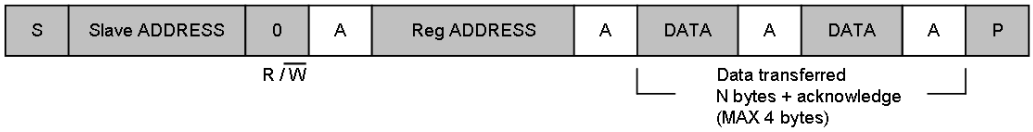


6.4 2 wire serial bus data transfer

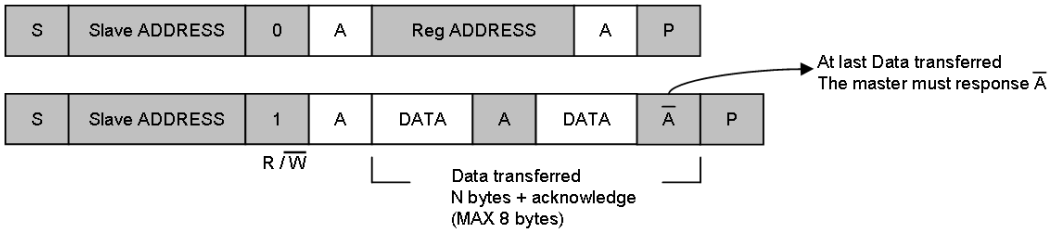


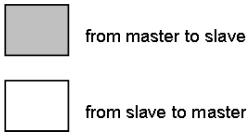
6.5 MCU 2 wire serial bus Read/Write

Set Data (Master write data to SSS1623)



Get Data (Master Read data from SSS1623)





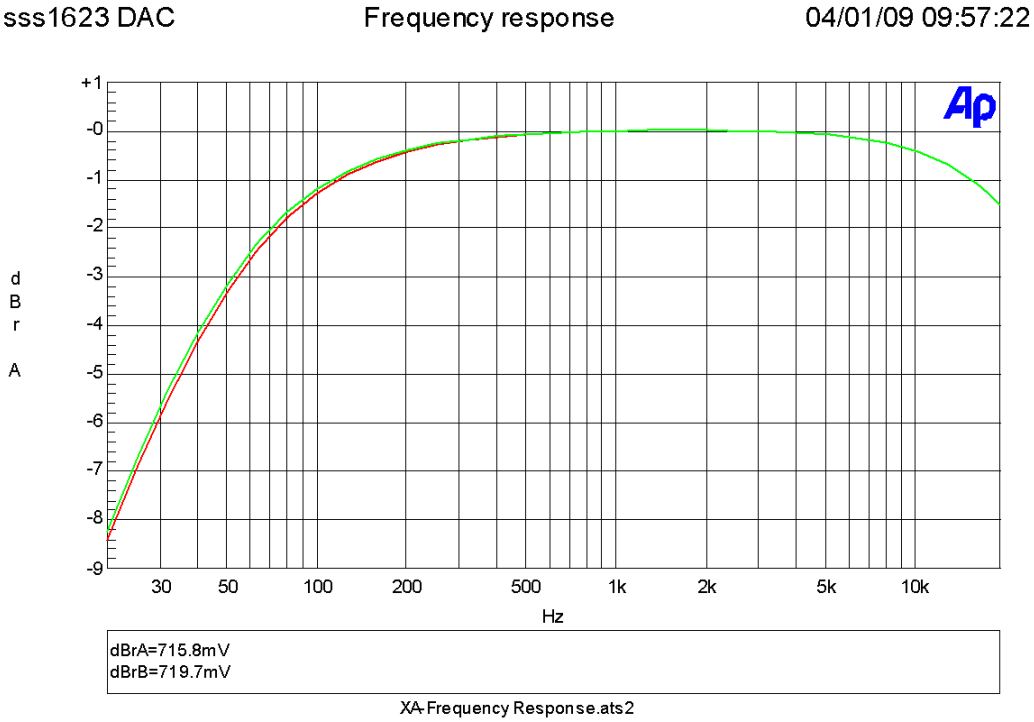
A = acknowledge (SDA LOW)
Ā = not acknowledge (SDA HIGH)
S = START condition
P = STOP condition
Slave ADDRESS = SSS1623 address : 3A (it can be modify by eeprom)
Reg ADDRESS = SSS1623 internal register address (0 - 7)
When Set MAX 4 bytes (0 - 3)
When Get MAX 8 bytes (0 - 7)

7. Typical Performance Curve

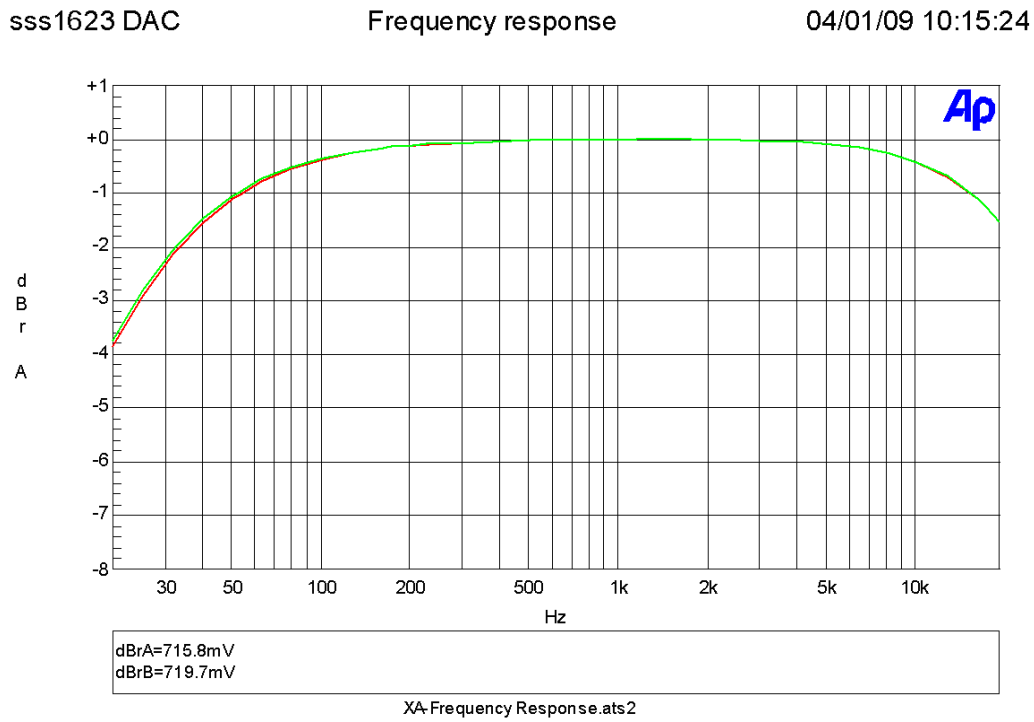
● DAC performance measurement

Frequency response

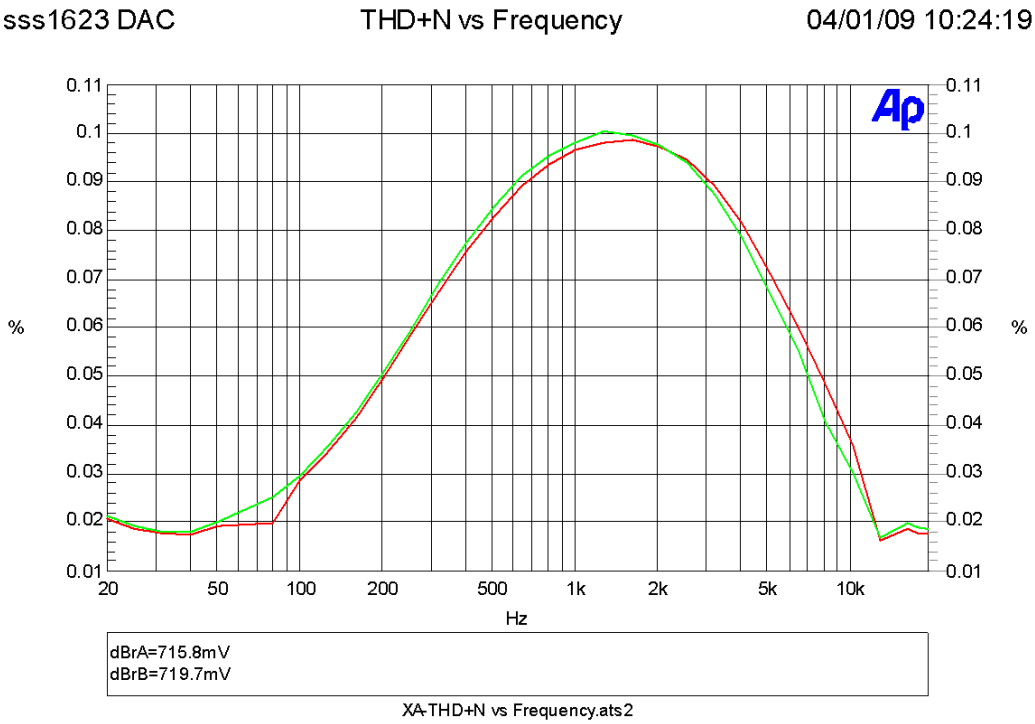
Blocking capacitor=100uF



Blocking capacitor=220uF



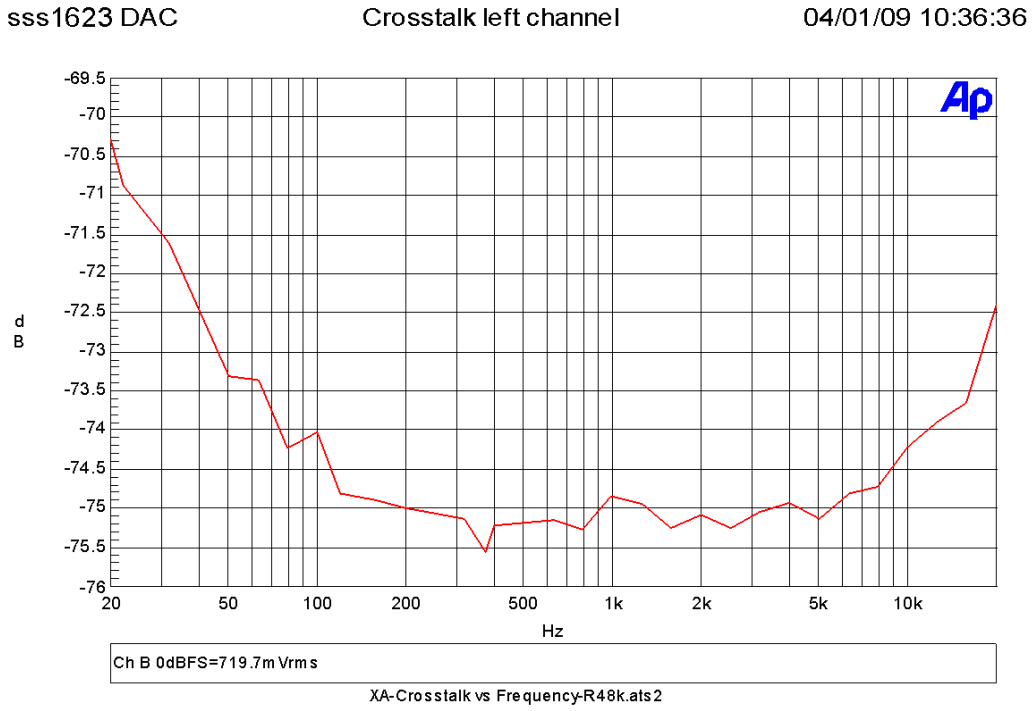
THD+N vs. frequency



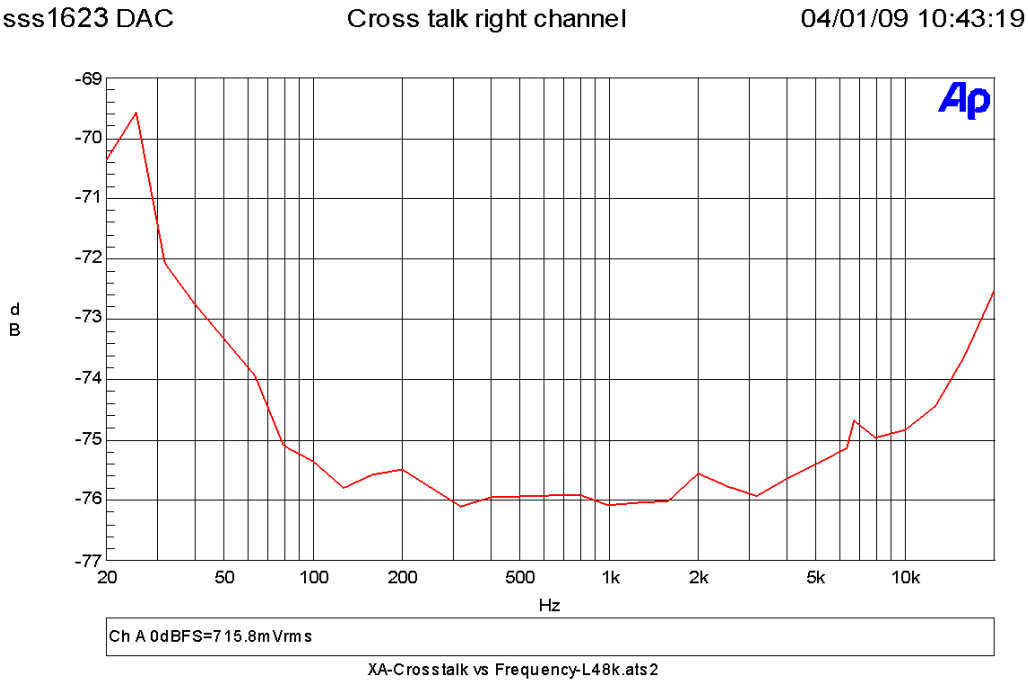
Crosstalk

Input signal: 20Khz→20hz sweep frequency,-20dB

Left channel

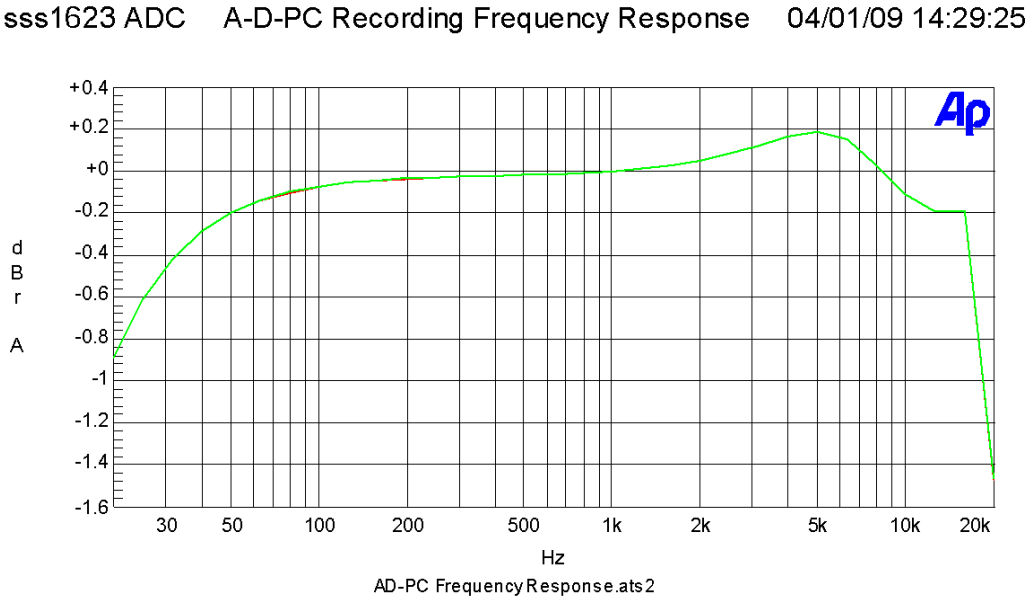


Right channel

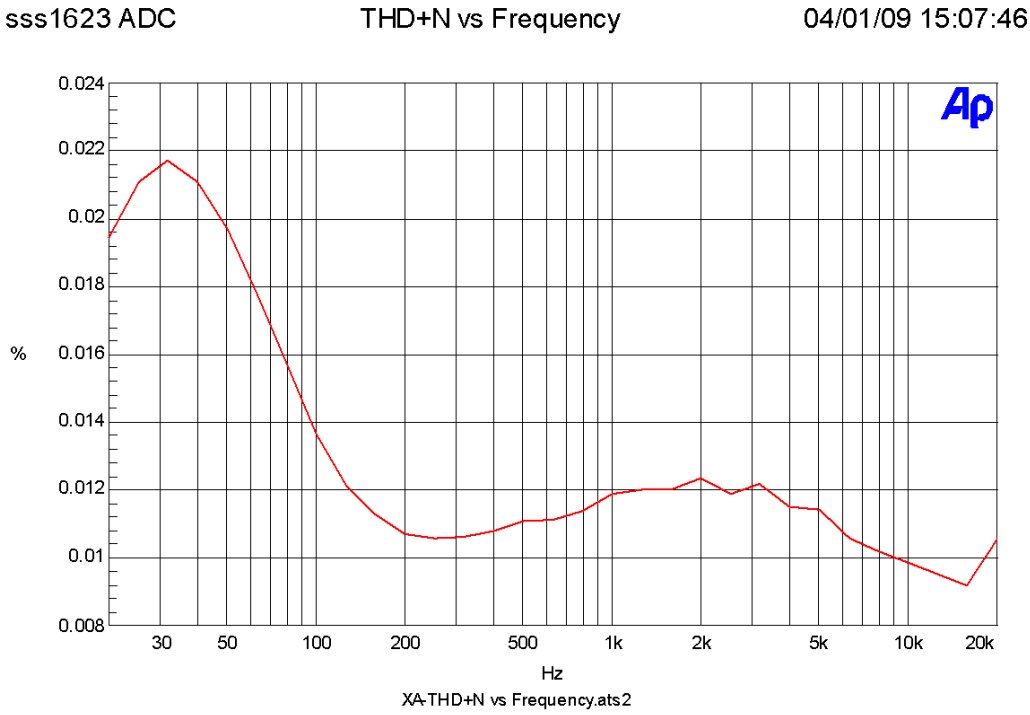


● ADC performance measurement

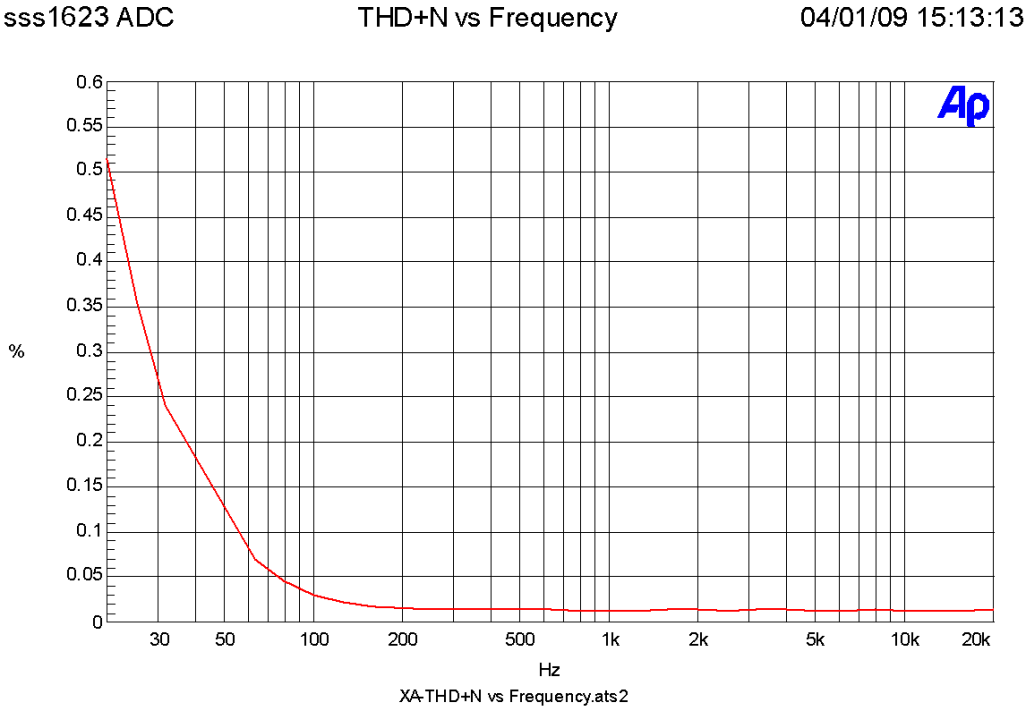
Frequency Response



THD+N v.s. frequency
Input signal:-3dB FS
With “a-weighting”



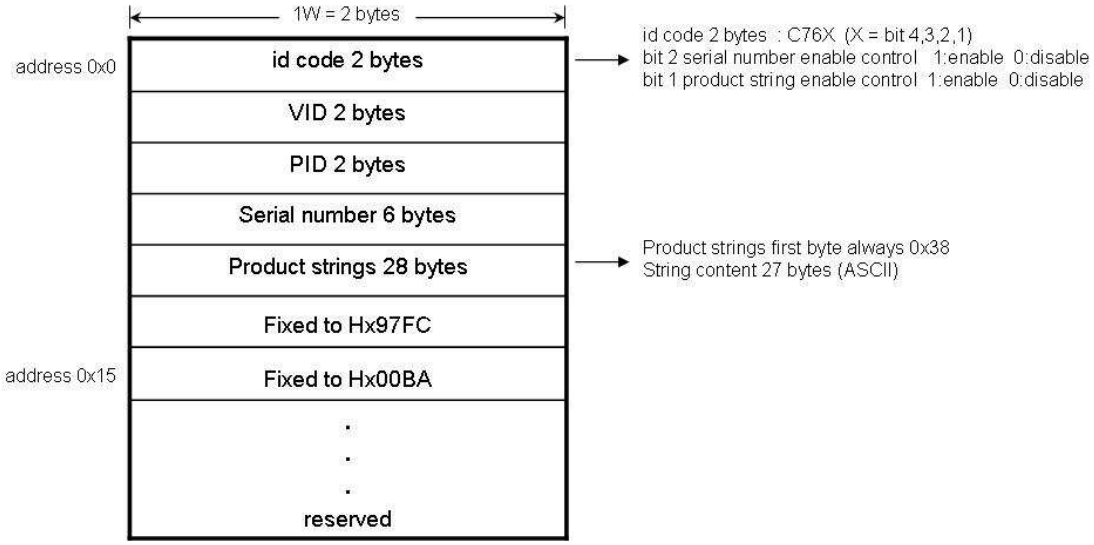
Without “a-weighting”



8. EEPROM Content and Descriptions

- **External EEPROM Setting**

EEPROM Setting



- **PLAY_EN & REC_EN Option**

PLAY_EN	REC_EN	function
0	0	Play only, support sampling rate : 48KHz
1	0	Play only, support sampling rate : 48KHz
0	1	Record only, support sampling rate : 8KHz, 11.025KHz, 22.05KHz, 32KHz, 44.1KHz, 48KHz
1	1	Play & Record (default), support sampling rate : 48KHz

- **Audio Path Gain Control**

Playback path gain control list

Playback path gain control list								
Parameter	**00**	**01**	**02**	**03**	**04**	**05**	**06**	**07**
Gain	0dB	-1dB	-2dB	-3dB	-4dB	-5dB	-6dB	-7dB
Parameter	**08**	**09**	**10**	**11**	**12**	**13**	**14**	**15**
Gain	-8dB	-9dB	-10dB	-11dB	-12dB	-13dB	-14dB	-15dB
Parameter	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**
Gain	-16dB	-17dB	-18dB	-19dB	-20dB	-21dB	-22dB	-23dB
Parameter	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**
Gain	-24dB	-25dB	-26dB	-27dB	-28dB	-29dB	-30dB	-31dB
Parameter	**32**	**33**	**34**	**35**	**36**	**37**		
Gain	-32dB	-33dB	-34dB	-35dB	-36dB	Mute		

Record path gain control list

Record path gain control list								
Parameter	**00**	**01**	**02**	**03**	**04**	**05**	**06**	**07**
Gain	+22.5dB	+21dB	+19.5dB	+18dB	+16.5dB	+15dB	+13.5dB	+12dB
Parameter	**08**	**09**	**10**	**11**	**12**	**13**	**14**	**15**
Gain	+10.5dB	+9dB	+7.5dB	+6dB	+4.5dB	+3dB	+1.5dB	0dB

Digital mixer gain control list

Digital mixer gain control list								
Parameter	**00**	**01**	**02**	**03**	**04**	**05**	**06**	**07**
Gain	0dB	-1.2dB	-2.4dB	-3.6dB	-4.8dB	-6dB	-7.2dB	-8.4dB
Parameter	**08**	**09**	**10**	**11**	**12**	**13**	**14**	**15**
Gain	-9.6dB	-10.8dB	-12dB	-13.2dB	-14.4dB	-15.6dB	-16.8dB	-18dB
Parameter	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**
Gain	-19.2dB	-20.4dB	-21.6dB	-22.8dB	-24dB	-25.2dB	-26.4dB	-27.6dB
Parameter	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**
Gain	-28.8dB	-30dB	-31.2dB	-32.4dB	-33.6dB	-34.8dB	-36dB	Mute

Playback path gain control list for CS42L51

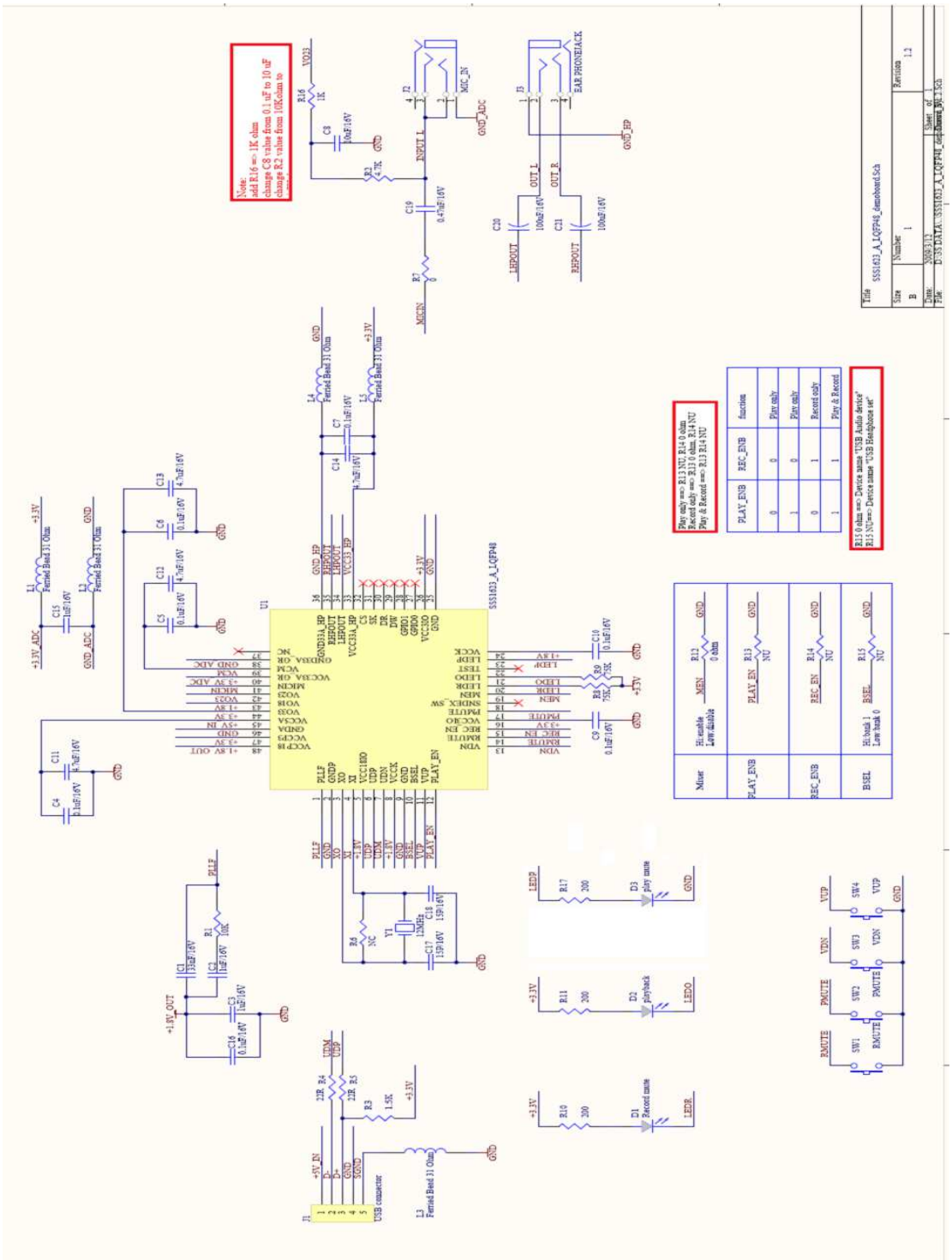
Playback path gain control list for CS42L51								
Parameter	**00**	**01**	**02**	**03**	**04**	**05**	**06**	**07**
Gain	0dB	-1dB	-2dB	-3dB	-4dB	-5dB	-6dB	-7dB
Parameter	**08**	**09**	**10**	**11**	**12**	**13**	**14**	**15**
Gain	-8dB	-9dB	-10dB	-11dB	-12dB	-13dB	-14dB	-15dB
Parameter	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**
Gain	-16dB	-17dB	-18dB	-19dB	-20dB	-21dB	-22dB	-23dB
Parameter	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**

Gain	-24dB	-25dB	-26dB	-27dB	-28dB	-29dB	-30dB	-31dB
Parameter	**32**	**33**	**34**	**35**	**36**	**37**		
Gain	-32dB	-33dB	-34dB	-35dB	-36dB	Mute		

Record path gain control list for CS42L51

Record path gain control list for CS42L51								
Parameter	**00**	**01**	**02**	**03**	**04**	**05**	**06**	**07**
Gain	+12dB	+11.5dB	+11dB	+10dB	+9dB	+8dB	+7dB	+6dB
Parameter	**08**	**09**	**10**	**11**	**12**	**13**	**14**	**15**
Gain	+5dB	+4dB	+3dB	+2dB	+1.5dB	+1dB	+0.5dB	0dB

9. Reference Application Circuits (LQFP 48 pin package)



Application circuit modification history:

1. Add R16 1K ohm;
2. Change C8 form 0.1uF to 10uF;
3. Change R2 from 10K ohm to 4.7K ohm

Note: This specification is subject to change without prior notice from 3S

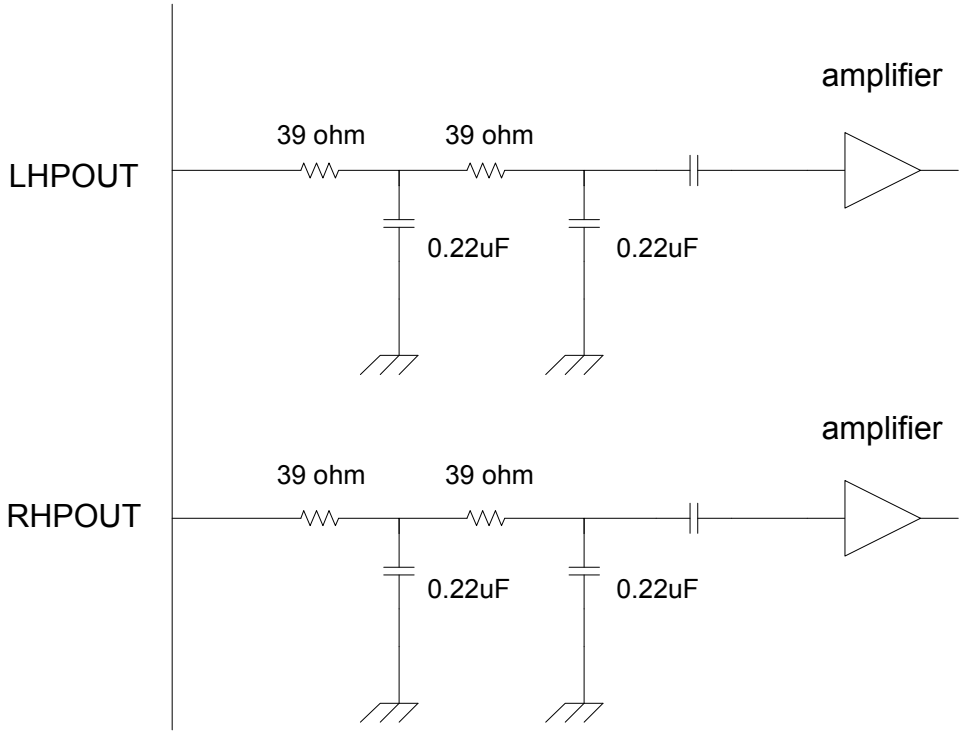
- **Outputs and External Filtering**

The delta-sigma conversion process produces high frequency noise beyond the audio passband, which can be attenuated using an off-chip low pass filter.

To achieve higher SNR, SSS1623's internal delta sigma DAC modulator pushes the in-band noise energy to high frequency out-band area. Although it is not audible, if users' application has the SSS1623's earphone amplifier driving an external light load component, for example, an amplifier line-in, the out-band noise might be folded back into in-band domain and causes audible noise during playback.

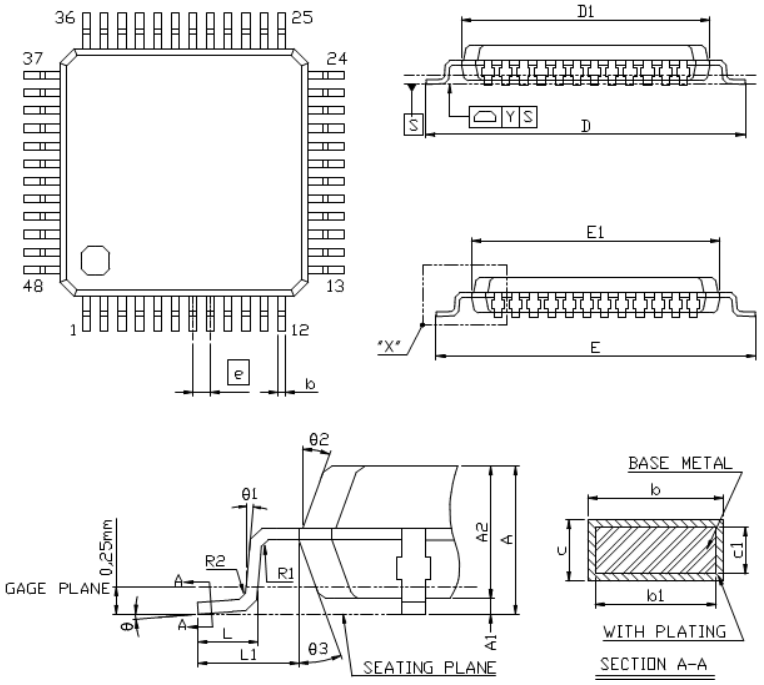
A simple RC low pass filter is recommended for this application. An example connection diagram is shown below. Different RC combination might be applied according to the characteristics of amplifier and speaker connected.

Such low pass filter is not required for earphone driving application.



10. Package Dimension

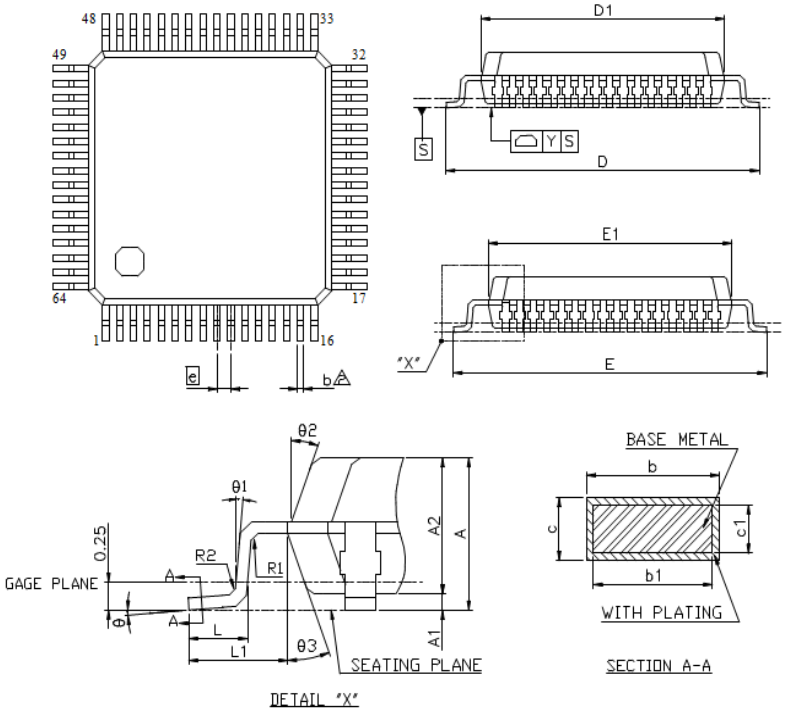
- **LQFP48**



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			63.0
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	1.35	1.40	1.45	53.1	55.1	57.1
b	0.17	0.22	0.27	6.7	8.7	10.6
b1	0.17	0.20	0.23	6.7	7.9	9.1
c	0.09		0.20	3.5		7.9
c1	0.09		0.16	3.5		6.3
D	8.90	9.00	9.10	350.4	354.3	358.3
D1	6.90	7.00	7.10	271.7	275.6	279.5
E	8.90	9.00	9.10	350.4	354.3	358.3
E1	6.90	7.00	7.10	271.7	275.6	279.5
e	0.45	0.50	0.55	17.7	19.7	21.7
L	0.50	0.60	0.70	19.7	23.6	27.6
L1	0.85	1.00	1.15	33.5	39.4	45.3
R1	0.08			3.1		
R2	0.08		0.20	3.1		7.9
Y			0.08			3.1
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°

NOTE:
1. REFER TO JEDEC MS-026 (ISSUE D) / BBC
2. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
   ALLOWABLE PROTRUSION IS 0.25mm PER SIDE D1 AND E1 ARE
   MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE
   DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED
   THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
4. ALL DIMENSIONS ARE IN MILLIMETERS.
5. DIMENSION CONVERSION FACTOR : 1mm=39.37mil

- **LQFP64**



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			63.0
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	1.35	1.40	1.45	53.1	55.1	57.1
b	0.13	0.18	0.23	5.1	7.1	9.1
b1	0.13	0.16	0.19	5.1	6.3	7.5
c	0.09		0.20	3.5		7.9
c1	0.09		0.16	3.5		6.3
D	8.85	9.00	9.15	348.4	354.3	360.2
D1	6.90	7.00	7.10	271.7	275.6	279.5
E	8.85	9.00	9.15	348.4	354.3	360.2
E1	6.90	7.00	7.10	271.7	275.6	279.5
e	0.35	0.40	0.45	13.8	15.7	17.7
L	0.45	0.60	0.75	17.7	23.6	29.5
L1	0.85	1.00	1.15	33.5	39.4	45.3
R1	0.08			3.1		
R2	0.08		0.20	3.1		7.9
Y			0.08			3.1
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°

NOTE:
1.REFER TO JEDEC MS-026(ISSUE D)/BBD
2.DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
ALLOWABLE PROTRUSION IS 0.25mm PER SIDE D1 AND E1 ARE
MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE
DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED
THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
4.ALL DIMENSIONS ARE IN MILLIMETERS.
5.DIMENSION CONVERSION FACTOR : 1mm=39.37mil

11.Revision History

Revision	Date	Description
1.2	2009/08/20	First release
1.3	2009/11/03	External low pass filter update
1.4	2010/02/04	Change product name from SSS1623 to SSS1623A3/A4 Errata : P3. Incorrect : Embedded digital Mixer Correct : Embedded digital Mixer (SSS1623A4 only) P7 Pin30 MEN_PAD Incorrect : Mixer enable 1: Enable Mixer 0: Disable Mixer Correct : SSS1623A3 : Tied to ground SSS1623A4 : Mixer enable 1: enable 0: disable P10 Pin19 MEN Incorrect : Mixer enable 1: Enable Mixer 0: Disable Mixer Correct : SSS1623A3 : Tied to ground SSS1623A4 : Mixer enable 1: enable 0: disable P12 Pin22 MEN Incorrect : Mixer enable 1: Enable Mixer 0: Disable Mixer Correct : SSS1623A3 : Tied to ground SSS1623A4 : Mixer enable 1: enable 0: disable
1.5	2011/12/23	Increased LQFP 32 pin chart and Application circuit's information
1.6	2012/12/06	Update ordering information
1.7	2014/09/10	Add performance curve and package information Modify format and text descriptions